FW V6.2

Time Slot Start

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDM ID				ID=0		Slot ID																		TDM TAG							

Spill header

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Spill header ID				Board ID							1	SId		DAQ type							Spill Time from GTRIG (10ns res.)										
Spill header ID				Board ID							0	SId				Spill tag (from reset request)															
Spill time ID				Spill time on spill start (10ms resolution, max=745.6 h=31 days)																											

GTRIG header #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTRIG header ID				Global Trigger tag (from reset request)																											

Event Data : Hit #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit time ID				Channel ID							Hit ID			Tag ID		EDGE				Hit time (2.5ns res.)											

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit Amplitude ID				Channel ID							Hit ID			Tag ID		Amplitude ID				Amplitude measurement											

...

Event Data : Hit #n

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit time ID				Channel ID							Hit ID			Tag ID		EDGE				Hit time (2.5ns res.)											

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hit amplitude ID				Channel ID							Hit ID			Tag ID		Amplitude ID				Amplitude measurement											

GTRIG trailer #1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTRIG trailer 1 ID				Global Trigger tag (from reset request)																											
GTRIG trailer 2 ID				Hit counts within gtrig*								Global Trigger time (10us res. % current spill start, max=10.5s)																			

Spill trailer

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Spill trailer ID				Board ID							0	SId				Spill tag (from reset request)															
Spill trailer ID				Board ID							1	SId		Temperature										Humidity							
Spill time ID				Spill time on spill end (10ms resolution, max=745.6 h=31 days)																											

Time Slot End

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDM ID				ID=1		Slot ID					21-bits CHECKSUM																				

Table 4 : TDM, GTRIG, SPILL & DATA structure for the FEB readout communication

IMPORTANT NOTICE: SPILL HEADER ID with bit20=0 for Spill Tag information can occur any time within [Spill header-Spill Trailer] due to delay of availability of the Spill Tag when using the external B-MIND triggering system (~800ns delay from spill gate)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Readout End																															
Special Word ID				Board ID							0	Special Word ID PARAM = 0x10000																			
GTRIG RESET																															
Special Word ID				Board ID							0	Special Word ID PARAM = 0x00001																			
SPILL RESET																															
Special Word ID				Board ID							0	Special Word ID PARAM = 0x00002																			
GTRIG + SPILL RESET																															
Special Word ID				Board ID							0	Special Word ID PARAM = 0x00003																			
FIFO FULL																															
Special Word ID				Board ID							0	Special Word ID PARAM = 0x00010																			
LOST of GTX WORD INTEGRITY																															
Special Word ID				0x00								Special Word ID PARAM = 0xF00FF																			

Table 5 : Special Word IDs structure for the FEB readout communication

Amplitude ID:

	HG	LG	HouseKeeping
COMPUTE	0000	0001	**0111***
COMPARE	0010	0011	0110
BASELINE	0100	0101	**0111***
OTHERS	**0111***	**0111***	**0111***

*: forbidden value (error)

Tag ID: 2 LSB: These bits are used for Tagging synchronization in order to place Timing & Amplitude measurement within the corresponding GTRIG event i.e. between its real Header/Trailer. The 2 LSB bits of the Tag ID must correspond to the current 2 LSB bits of the Global Trigger Tag. Due to the different clock domains and the FIFOs cascade latency used for the readout, the hit or amplitude ID message may be sent on the next GTRIG header/trailer cell if the event occurs just before the GTRIG signal. Moreover the probability of having an amplitude event on the next GTRIG is higher since it takes ~9us to process the analog readout (ASIC LG/HG multiplexed outputs) compared to an hit event which is pushed in the readout flow within 10-20ns due to FIFO to FIFO shorter latencies (2.5ns clocking).

Hit ID: 3 bits: these bits are used to synchronize the Amplitude event with the corresponding Timing event. Indeed, the amplitude measurement takes approximatively ~9s while several timing events can be latched and sent during this lapse. As soon as a Time event occurs on a given channel, the analog stage latches the hit ID of this channel and this latch is enabled during the entire HOLD DELAY duration and the ADC reading is started at the end. In other words, if many channels are hit the time flow, the corresponding analog ones will be associated with the Hit ID bits field since both timing & analog flows tag the same Hit ID. A rollover counter of 8 events (3-bits) is used.

EDGE: used for hit timing identification of event: 0=rising edge of event, 1=falling edge of event. The event duration may be calculated with the difference of the falling and the rising edge time stamps.

Channel ID: the channel IDs are used for the HG/LG identification but also for the Housekeeping channels identification. In this particular case, Channel number is equivalent to:

CH	SIGNAL	CONVERSION
0	TEMPERATURE ASIC 0	
1	TEMPERATURE ASIC 2	
2	NC	
3	TEMPERATURE ASIC 1	
4	TEMPERATURE FPGA	T(°C) = ADC(LSB)-128
5	GLOBAL HV	HV(V) = ADC(LSB)*822E-6*(1+1000/41.2)
6	BOARD TEMPERATURE	T(°C) = -(ADC(LSB)*822E-6 – 2.633)*1000/13.3
7	BOARD RELATIVE HUMIDITY[§]	RH(%) [¤]= (ADC(LSB)*822E-6/3.3 – 0.1515)/0.00636 True RH (%) = RH(%)/(1.0546-0.00216T(°C))

[§] If sensor U52 is mounted, else ADC(LSB) = 0 i.e. HR=-23.8%. RH(%) is not compensated in temperature, use True RH formula with Board temperature measurement for temperature compensated RH(%).

SiD: Sub Board ID is an additional optional identification set by the slow control FPGA software configuration (e.g. vertical/horizontal separated identification)

DAQ Type: 3-bits DAQ type composed of bits 15(LSB) to 17(MSB). This field is set by the MCB depending of the MCB DAQ mode and can have the following values:

000*: None*
001*: 60us Beam DAQ pulse on external on external NIM input 0*
010*: Internal DAQ (20ms after Beam DAQ, duration=1.966s) on external NIM input 0*
011*: 001 OR 010 modes (i.e. 2 pulses) on external NIM input 0*
100*: 1.986s full pulse on external NIM input 0*
101*: Wagasci mode with 1x60µs Beam DAQ pulse + 6x5ms DAQ pulses on HDMI input*
110: *External NIM input 1(direct level)*

NB: when using the FEB MCB emulation, the FEB can send only one DAQ type which is '001'.

R: Reserved bit (=0)
Special Word ID:

The bit-20 is used for defining the sub-special ID:
- 0: The 20-bits LSB (bits[19..0]) define the Special Word ID parameter :
  - 0x10000: END of readout. In that case, bits [27..21] corresponds to board ID.
  - 0x00001: GTRIG RESET received. In that case, bits [27..21] corresponds to board ID.
  - 0x00002: SPILL RESET received. In that case, bits [27..21] corresponds to board ID.
  - 0x00003: GTRIG + SPILL RESET received. In that case, bits [27..21] corresponds to board ID.
  - 0x00010: FIFO L2 Full. In that case, bits [27..21] corresponds to board ID.
  - 0xF00FF: Lost of GTX Word integrity. Board ID = 0 in this case having a global word 32 = 0xF00F00FF
- 1: Unused

TDM Word ID:
- The bits 27 & 26 are now defining sub-time slot ID:
  - '00' for Time slot START. : In that case :
    - Bits [25..21] define the slot ID encapsulating the board data associated to this time slot.
    - Bits [7..0] define the TDM Tag which is incremented by 1 on every new TDM start and with a 8-bits rollover counter
  - '01' for Time Slot END: In that case :
    - bits [25..21] define the slot ID encapsulating the board data associated to this time slot
    - bits [20..0] is the 32-bits to 21-bits truncated Fletcher checksum computed for the overall data sent within the time slot (**including** 'Timeslot Start' **BUT excluding** 'Time slot End' 32-bits words).

Fletcher checksum algorithm:
At every TDM slot start:
```
UInt32 checksumL = 0;
UInt32 checksumH = 0;
```

At every 32-bits data frame sent within the time slot:
```
checksumL = checksumL + data;
checksumH = checksumH + chksumL;
```

At every TDM slot end:
```
checksum_sent = ((checksumH & 0x3FF)<<11) & (checksumL & 0x7FF); // 10-bits checksum Hi + 11-bits Lo
```