# **FASER PRE-SHOWER** V1.3 => V1.4 GUI & Firmware Interface changes

# 1 Direct Parameters



- 1- **PLL\_Auto\_Set** bit (bit[1]) becomes **PLL\_Scan** to start a scan of the connected modules ASICs phases (Module must be configured in oscillator mode before to start the scan)
- 2- **PLL\_Apply** is a new bit (bit[12]) to apply the phase configuration:
  - a. If PLL\_Scan bit is set at the same time than PLL\_Apply bit, the scan will be done and finally the PLL will be set with the result of the scan (same behaviour than previous single bit PLL\_Auto\_Set
  - b. If only PLL\_Apply bit is set, the PLL will be set with the phase values configured in the new TAB **Phase.PhaseSet** (see below §4)
- ⇒ DAQ I/F must add the new PLL\_Apply bit (mapping for other bits remains the same)
- $\Rightarrow$   $\:$  Need to update GUI scripts for PLL\_Scan, and add new PLL\_Apply bit  $\:$

## 2 Tab Renaming

- 1- TEST\_OUT becomes ModuleConfig for CHIP\_CONFIG\_M0..M5 and SPI\_START
- 2- TEST\_OUT becomes General for RO\_PARAM

#### ⇒ Need to update GUI scripts:

- TEST\_OUT.CHIP\_CONFIG\_M0 => ModuleConfig.CHIP\_CONFIG\_M0
- TEST\_OUT.RO\_PARAM => General.RO\_PARAM

#### ⇒ No changes in DAQ I/F for variable addressing (just renaming)

Board M0 M1 M2 M3 M4 M5 Modu	leConfig General Phase										
CHIP_CONFIG_M0	CHIP_CONFIG_M2	CHIP_CONFIG_M4	SPI_START								
Update	Update	Update	Update								
Copy CHIPADDRESS0 to others	Copy CHIPADDRESS0 to others	Copy CHIPADDRESS0 to others	CHIP_CFG_EN_M0								
CHIP_ADDRESS #0 #1 #2 #3 #4 #5	CHIP_ADDRESS #0 #1 #2 #3 #4 #5	CHIP_ADDRESS #0 #1 #2 #3 #4 #5	CHIP_CFG_EN_M1								
			CHIP_CFG_EN_M2								
0 SPI_DATA	0 SPI_DATA	0 SPI_DATA	CHIP_CFG_EN_M4								
0 CHIP_ADDRESS	0 CHIP_ADDRESS	0 CHIP_ADDRESS	CHIP_CFG_EN_M5								
0 SUPER_COLUMN_NB	0 SUPER_COLUMN_NB	0 SUPER_COLUMN_NB									
0 SEL	0 SEL	0 SEL									
CHIP_CONFIG_M1	CHIP_CONFIG_M3	CHIP_CONFIG_M5	CHIP_CONFIG_M5								
Update	Update	Update									
Copy CHIPADDRESS0 to others	Copy CHIPADDRESS0 to others	Copy CHIP <u>A</u> DDRESS0 to others									
CHIP_ADDRESS #0 #1 #2 #3 #4 #5 SC_NRESET V V V V V	CHIP_ADDRESS #0 #1 #2 #3 #4 #5 SC_NRESET 🗸 🗸 🗸 🗸	CHIP_ADDRESS #0 #1 #2 #3 #4 #5 SC_NRESET 🗸 🗸 🗸 🗸									
0 SPI_COMMAND	0 SPI_COMMAND	0 SPI_COMMAND									
0 SPI_DATA	0 SPI_DATA	0 SPI_DATA									
0 CHIP_ADDRESS	0 CHIP_ADDRESS	0 CHIP_ADDRESS									
0 SUPER_COLUMN_NB	0 SUPER_COLUMN_NB	0 SUPER_COLUMN_NB									
0 SEL	0 SEL	0 SEL									

## 3 New RO\_PARAM

New readout parameters for internal 10us generator:

- 10US\_L1A\_GEN\_EN: enable internal L1A generator, bit[15]
- 10US\_L1A\_GEN\_PERIOD: set period for L1A generator (10-bits coding, 10µs step, 0:10µs, max=1023:10.24ms, period = (value+1)=10µs), bit[14..5]

In order to enable the generator, the direct parameter 'Autotrig\_(no\_L1A)' (bit[2]) must be enabled as well as the '10US\_L1A\_GEN\_EN' above.

NB: WINDOW\_DURATION remains the same (bit[4..0])



**WARNING:** WINDOW\_DURATION, 10US\_L1A\_GEN\_EN and 10US\_L1A\_GEN\_PERIOD must **NEVER** be changed during run.

# 4 New Phase Tab

Added new tab for PhaseSet and PhaseGet:

- 1- **PhaseSet** is a 36 x 5-bits array used to set the phase of each chip individually (used when Apply mode only (PLL\_Apply bit =1 and PLL\_Scan bit = 0)
- 2- **PhaseGet** is a 36 x 5-bits array used to get the phase of each chip individually. The result depends on the previous action made:
  - a. **Apply mode only:** (PLL\_Apply bit =1 and PLL\_Scan bit = 0) the **PhaseGet** values corresponds to the PLL setting
  - b. **Scan + Apply mode:** (PLL\_Apply bit =1 and PLL\_Scan bit = 1) the **PhaseGet** values corresponds to the PLL setting
  - c. Scan mode only (Not recommended): (PLL\_Apply bit =0 and PLL\_Scan bit = 1) the **PhaseGet** values corresponds to the result of the scan, the PLL remains with the last phase scan i.e. phase = 31 for all the chips. It is not possible to work with the chip(s) properly at the end of this phase

#### ⇒ DAQ I/F must add this new layout

**Important:** In order to retrieve the proper phase values before to launch an 'apply only' command, you must perform at least 1 scan in the 1 of the following conditions:

- New module never scanned
- Pig tail length change for an already scanned
- New firmware version

A new '**PhaseSet**' device has been added so the GUI configuration can be saved and recalled for the phase values to set.

Config	urati	on –										
	Star	t	۲	Send, Verify & Apply Devices:								
	Verit	iv.	0	Send	d Onl	у		$\checkmark$	] M0	$\checkmark$	M4	
	veni	у	0	○ Valid World Only				M1	$\checkmark$	M5		
	Rea	d						$\checkmark$	M2	$\checkmark$	PhaseSet	1
												1
E. 105												
Board	M0	M1	M	2 1	13 N	<b>/</b> 4	M5	Mod	uleCo	nfig	Genera	Phase
Config	ure A	II										
PhaseSe	et —											
Config	ure T	his										
Сору	CHI	PO to	others	5								
CHIP	#0	#1	#2	#3	#4	#5	#6	#7	#8			
Phase	0	0	0	0	0	0	0	0	0			
CHIP	#9	#10	#11	#12	#13	#14	#15	#16	#17			
Phase	0	0	0	0	0	0	0	0	0			
CHIP	#18	#19	#20	#21	#22	#23	#24	#25	#26			
Flidse	0	0	0	0	0	0	0	0	0			
CHIP	#27	#28	#29	#30	#31	#32	#33	#34	#35			
Phase	0	0	0	0	0	0	0	0	0			
PhaseG	et —											
Update	•											
CHIP	#0	#1	#2	#3	#4	#5	#6	#7	#8			
Phase	0	0	0	0	0	0	0	0	0			
CHIP	#9	#10	#11	#12	#13	#14	#15	#16	#17			
Phase	0	0	0	0	0	0	0	0	0			
CHIP	#18	#19	#20	#21	#22	#23	#24	#25	#26			
Phase	0	0	0	0	0	0	0	0	0			
CHIP	#27	#28	#29	#30	#31	#32	#33	#34	#35			
PridSe	0	0	0	0	0	0	0	0	0			